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Alayne Geller

6/19/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of Bao *et al.*	
Serial No.: 09/305,722	Group Art Unit: 1746
Filed: May 5, 1999	Examiner: R.P. Gulakowski
For: HIGH-RESOLUTION METHOD FOR PATTERNING A SUBSTRATE WITH MICROPRINTING	

BRIEF OF APPELLANTS FROM
FINAL REJECTION OF SEPTEMBER 28, 2002

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Applicants Zhenan Bao *et al.* respectfully appeal the Final Rejection mailed October 4, 2002 of their above-identified application.

Real Party in Interest

The real party in interest is Agere Systems Inc., the assignee of Applicants' interests in this invention.

Related Appeals and Interferences

There are no other appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims

Applicants appeal the final rejection of claims 1, 3-5, 7-9, 11, 12, and 19. Claims 13-15 and 20-22 have been withdrawn from consideration as directed to non-elected species. No claims have been allowed. The appealed claims are set forth in an attached Appendix.

Status of Amendments

An amendment after final rejection was filed February 13, 2003, but the Examiner declined to enter it.

Summary of the Invention

Applicants' invention is a method of forming a patterned layer on a substrate particularly useful for the fabrication of organic semiconductor devices such as organic transistors. Applicants' specification teaches that conventional methods for patterning semiconductor substrates are inapplicable to the fabrication of organic semiconductor devices (p. 2, line 20 - p. 3, line 10). While micromolding processes have been adapted for the fabrication of organic transistors, these processes are slow, incompatible with efficient reel-to-reel processing and not readily applicable to the formation of dense circuitry (p. 3, lines 11-21).

The specification teaches that these problems can be overcome by a novel process comprising providing a rotatable stamp with a relief geometry surface, applying an ink to the

surface of the rotatable stamp, rotating the stamp in contact with a substrate to form inked patterns of self-assembled monolayers on the substrate, using the inked pattern to guide etching and then removing the inked pattern.

The specification further teaches the use of inking materials comprising substances known to form self-assembled monolayers when applied to particular substrate materials, such as alkanethiol or alkylsiloxane. (Specification, p. 7, lines 10-15). For example, the specification discloses the use of "inks of alkanethiols . . . to define monolayer etch resists on surfaces of thin films of gold or silver." (Specification, p. 11, lines 1-2).

Various stages of an exemplary embodiment are illustrated in Figs. 2A through 2D. Fig. 2A shows an inked rotatable stamp 10 rotating over a substrate 14 including a surface layer 16. Fig. 2B illustrates the inked pattern impressed on the substrate surface to protect an underlying region 20, leaving the remaining region 18 of the substrate surface exposed. Fig. 2 shows that the exposed region 18 has been etched away, and Fig. 2D illustrates the ink pattern removed, revealing the unetched protected region. An important advantage of this process is that it permits reel-to-reel fabrication of electronic components as illustrated in Fig.7.

This is essentially the process recited in claim 1. Claims 3-5, 7-9, 11, 12, and 19 depend from claim 1.

Issues

The issues for resolution are:

(1) whether claims 1, 3-5, 7-9, 11, 12, and 19 as amended contain "new matter" that was not disclosed at the time the application was filed and are therefore unpatentable under 35 U.S.C. §112, first paragraph; and

(2) whether those same claims are unpatentable under 35 U.S.C. §103 in view of the Xia *et al.* publication, "Microcontact Printing With A Cylindrical Rolling Stamp", either alone or in combination with Kumar *et al.*, United States Patent No. 5,512,131, or Tanaka *et al.*, United States Patent No. 6,060,338.

Grouping of Claims

The claims stand or fall together. Claim 1 is the only independent claim, and the Examiner's rejection was directed to the language of that claim.

Argument

1. Rejection Based on 35 U.S.C. §112, First Paragraph

Applicants respectfully submit that the Examiner's rejection of Applicants' amended claims based on §112 is without basis. Specifically, the Examiner identified as "new matter" the limitation "applying a self assembled monolayer ink to the surface of a rotatable stamp." Although the Examiner acknowledged that the specification recites the use of inks that are comprised, for example, of alkanethiol, the Examiner erroneously interpreted Applicants' claim, stating:

> There is no mention of this ink being a monolayer, nor of it being a self-assembled monolayer. A SAM forms on the gold surface when the stamp is imprinted on the gold. There is no description of forming a SAM on the stamp.

Of course, the Examiner is entirely correct that the specification provides no description of forming a self-assembled monolayer on the stamp, because that is not the Applicants' invention. Nor is it claimed. Applicants' invention consists in part of applying to an elastomeric or other type of stamp an ink containing a compound such as alkanethiol that is known to form self-assembled monolayers when applied to metals. The inked stamp is then used to print a self-assembled monolayer pattern on a thin metal layer.

Applicants' claim 1 does not claim forming a self-assembled monolayer on the stamp, as the Examiner misunderstood. Apparently, the Examiner misunderstood the claim term "self assembled monolayer ink" to mean an ink that acts in isolation from any surface as a self-assembled monolayer, and would also act as such a monolayer when applied to the stamp. Persons skilled in the art, however, understand that the formation of a self-assembled monolayer requires the application of an organic compound, for example an alkane chain, that has a preferential adsorption affinity matched to the desired substrate, such as a gold film, and would

further understand that the claim term "self assembled monolayer ink," as used in microlithography, refers to an ink that forms such a monolayer when applied to a proper substrate, such as the well-known combination of alkanethiol applied to gold or silver.

That the "ink" claimed by Applicants is intended to form the self-assembled monolayer on the substrate, as opposed to the stamp, is made clear by Applicants throughout the specification. *See* Specification p. 6, lines 4-5 ("Elastomeric stamps and inks may be used to print patterns of self assembled monolayers (SAMS) onto a substrate . . ."); p. 8, lines 7-9 ("When the substrate is placed in contact with the inked stamp (FIG. 1, block 3), an inked pattern, e.g., a patterned self-assembled monolayer (SAM) 20 is imprinted on the surface of the substrate."); p. 11, lines 1-2 ("in applying this technique inks of alkanethiols are used to define monolayer etch resists on surfaces of thin films of gold or silver").

Accordingly, the Examiner's "new matter" rejection of claims 1, 3-5, 7-9, 11, 12, and 19 is without basis. Although Applicants do not believe any further clarity is required in the claim language, to the extent that the Board desires, Applicants are willing to amend claim 1 as may be necessary to make clear that the "self assembled monolayer ink" is a "self-assembled monolayer-forming ink" that forms such a monolayer on the substrate. As noted above, such claim language is fully supported by the specification.

2. Rejection Based on 35 U.S.C. §103

Although there is no separate heading in the Final Rejection directed to obviousness, and no citation to §103, the Examiner appears also to have based the final rejection on §103. Specifically, the Examiner stated that:

> [T]he new limitation [added to claim 1] of applying an organic semiconductor layer is obvious. Xia discloses an intermediate product, for which further processing is obvious, such as forming layers for known electronic devices such as organic transistors (see Tanaka et al., U.S. Patent No. 6,060,338). Also note that Kumar discloses to form an organic polymer, which encompasses an organic semiconductor layer (claim 37).

These comments were in response to Applicants' amendment to claim 1 to add the method step of "applying an organic semiconductor layer overlying the etched metal layer."

This step was added to distinguish over Xia in view of Kumar. Kumar discloses the use of a planar stamp to apply a self assembled monolayer to a metal film, and further discloses the removal of the self assembled monolayer, but neither Xia nor Kumar teach the application or use of organic semiconductive layers to a metal film after removal of a self-assembled monolayer.

Neither Xia nor Kumar, individually or in combination, render obvious the invention of claim 1. For a reference or a combination of references to make obvious a claimed invention, the references must teach or suggest all the claim limitations. See *In re Chu*, 66 F. 3d 292, 36 USPQ 2d 1089, 1094 (Fed. Cir. 1995). Moreover, if the references must be modified or combined to make obvious the claimed invention, there must be some teaching or motivation in the references which suggests the modification or combination. See *In re Fritch*, 972 F. 2d 1260,1266; 23 USPQ 2d 1780 (Fed. Cir. 1992):

> The mere fact that the prior art may be modified as suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.

In the present case, Xia *et al.* discloses a microcontact printing process. It is devoid of the claimed step of "removing the inked pattern from the substrate." Although the Examiner stated that subjecting the etched substrate to "further processing" is "obvious," the Examiner cites no reference other than Kumar and Tanaka to support the Examiner's apparent conclusion that it would be obvious to conduct "further processing" consisting of removing the self-assembled monolayer film from the substrate and then adding an organic semiconductor layer, as claimed by Applicants in claim 1 as amended.

Tanaka is directed to the fabrication of organic transistors, but does not teach the use of microlithography, self-assembled monolayer resists, or etched metal layers. In short, Tanaka has little relation to Applicants' invention other than that it discloses the use of semiconductive polymers to make organic transistors.

Xia, moreover, teaches away from the method step of Applicants' invention of removing the self-assembled monolayer. The removal step, Applicants discovered, is needed to enable good connections between the patterned metal layer and other components, such as gold electrodes. See p. 9, lines 9-10. Literature in the organic transistor art, however, teaches that the

self-assembled monolayer should be left on the metal surface layer after etching. This is demonstrated by the primary reference to Xia et al. which leaves the self-assembled monolayer patterns in place (see Xia, Fig. 1). Corroboration of Applicants' position is further provided in the article by Kymisses, "High-Performance Bottom Electrode Organic Thin-Film Transistors", 48 *IEEE Trans. On Electron Devices*, No. 6, pp.1060-1064, which was made of record when Applicants filed a previous Appeal Brief, mailed July 25, 2001. (For the convenience of the Board, a copy of this article is attached. See particularly, p. 1062 under Experimental Procedure. Also see p. 1064, 1st column, first full paragraph.

The Examiner stated that Kumar "discloses to form an organic polymer, which encompasses an organic semiconductor layer (claim 37)." Claim 37 of Kumar, however, is indefinite, because it depends from claim 1 of that patent, and the layer onto which the polymer is coated is recited as "said at least one second material surface." There is no antecedent basis for the "second material surface," either in claim 1, any other claim, or anywhere in the specification of the Kumar patent. Therefore, the teaching, if any, of claim 37 of Kumar is not ascertainable.

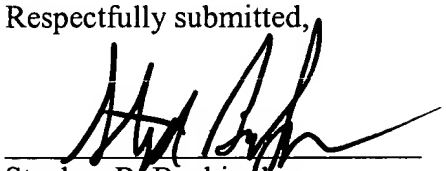
Even aside from its indefiniteness, under any reasonable guess at the meaning intended for claim 37 in Kumar, that claim does not teach adding an organic semiconductor layer, or any layer, for that matter, to an etched metal surface from which a self-assembled monolayer has been removed. Rather, claim 37 appears to teach forming a conductive, not semiconductive, polymer layer on a surface, and then removing the self-assembled monolayer "to uncover said conductive polymer." It therefore appears that claim 37 may teach the use of a conductive polymer, instead of a metal layer, from which a self-assembled monolayer has been removed, but nowhere discloses the application of an organic semiconductor layer over the conductive polymer.

In sum, neither Xia, nor Tanaka, nor claim 37 of Kumar nor any other claim or disclosure in the specification of Kumar discloses the application of an organic semiconductor to an etched metal layer, and Xia and other art teaches away from the removal of the self-assembled monolayer film in the production of organic semiconductor devices. Thus the references cannot be combined, even if there were a suggestion to do so, to render Applicants' claims obvious.

Accordingly claim 1 as amended and its dependent claims patentably distinguish over Xia, Tanaka and Kumar.

In view of the foregoing, the final rejection of claims 1, 3-5, 7-9, 11, 12, and 19 are without basis, and should be REVERSED.

Respectfully submitted,



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APPENDIX

What is claimed:

1. A method for forming at making an organic transistor on a substrate comprising the steps of:

providing a substrate including a metal surface layer;

providing a rotatable stamp having relief geometries on its surface to define a stamping surface;

applying a self-assembled monolayer ink to the surface of the rotatable stamp to define an inked stamping surface;

rotating the rotatable stamp on the metal surface layer as the layer is placed in contact with the stamp to impress on the layer an inked pattern as defined by the inked stamping surface; and

patterning the layer by etching material from the layer wherein the inked stamping surface guides the etching in a geometry to define the patterned layer useful in fabricating an electronic device;

removing the inked pattern from the layer; and

applying an organic semiconductor layer overlying the etched metal layer.

3. The method of claim 1, in which the step of providing the rotatable stamp comprises:

(a) casting a liquid onto a surface having relief geometries thereon;

(b) solidifying the liquid to define a solid film; and

(c) rolling a member over the solid film so that the solid film is lifted from the surface and bonds to the member.

4. The method of claim 3, in which the liquid comprises an elastomeric material, the step of solidifying the liquid comprises curing the elastomeric material to form an elastomeric film.

5. The method of claim 4, further comprising a step of exposing the cured elastomeric film to oxygen plasma before the member is rolled over the film.

7. The method of claim 6 in which the at least one coating layer includes a thin layer of gold or silver.

8. The method of claim 1 in which the step of patterning the metal layer comprises etching material from the substrate applying an etchant selected from the group consisting of aqueous ferrocyanide, $K_4Fe(CN)_6$, $K_3Fe(CN)_6$, $Na_2S_2O_3$, and KOH in H_2O.

9. The method of claim 1, in which the step of rotating the stamp provides an exposed region on the metal layer where substantially no ink is present and a protected region on the layer where ink substantially covers protected region.

11. The method of claim 10, in which the metal layer has an applied adhesive layer selected from the group consisting of Ti and Cr.

12. The method of claim 1 in which the inked pattern is removed by ultraviolet light, heat, or wet chemical cleaning.

19. The method of claim 3 wherein the member comprises a cylinder with a glass surface.

High-Performance Bottom Electrode Organic Thin-Film Transistors

Ioannis Kymissis, *Student Member, IEEE*, C. D. Dimitrakopoulos, and Sampath Purushothaman

Abstract—**Pentacene-based organic field effect transistors (FETs) exhibit enormous potential as active elements in a number of applications. One significant obstacle to commercial application remains: no completely lithographic process exists for forming high-performance devices. Processing constraints prevent electrodes from being lithographically patterned once the semiconductor is deposited, but depositing the electrodes before the semiconductor leads to low-performance transistors. By using self-assembled monolayers (SAMs) to change the surface energy of the metal electrodes and morphology of the pentacene subsequently grown on the electrodes, high-performance transistors may be formed using a process compatible with lithographic definition of the source and drain electrodes.**

Index Terms—**Contacts, organic compounds, thin film transistors.**

I. Introduction

ORGANIC semiconductors, and the organic semiconductor pentacene in particular (Fig. 1), have attracted considerable interest for use in a number of applications including large-area flat panel displays, radio frequency identification tags, and smart cards. Significant improvements have been made in the performance of these materials through the optimization of deposition parameters, material purification, and optimized design of device and gate geometry. Mobility values from test devices with pentacene active layers are adequate for use in these applications and are comparable to amorphous silicon [1]. Furthermore, the use of relatively high dielectric constant gate insulators results in low operating voltages without compromising mobility [2]. Processing these devices is, however, difficult. Pentacene is intolerant to exposure to solvents and other liquids [3] and this has limited its commercialization potential to date by eliminating photolithographic techniques from defining the semiconductor layer and contacts deposited after the semiconductor. Pentacene transistor drain-source contacts can be made in one of two configurations (Fig. 2)—top contact and bottom contact. It has been demonstrated that the bottom contact configuration gives inferior performance to the top contact configuration for a range of deposition conditions and material thickness [4], [5]. As a consequence of this behavior, the top contact configuration is almost exclusively studied and reported in the literature. Shadow masking is generally used in the laboratory to define the top contacts made to pentacene, a procedure which does not lend itself well to manufacturing.

To create a manufacturable process photolithographically defined drain and source contacts are needed. The performance levels needed for commercial technologies have only been demonstrated in top contact devices, however, and since no photolithography may be performed after pentacene has been deposited, bottom contact devices are the only option for a fully lithographic pentacene process. This paper will present a technique for achieving performance comparable to top contact FET devices using a bottom contact process, enabling a high-performance pentacene process with lithographically defined source and drain electrodes. This removes one of the two remaining obstacles to a high-performance, fully lithographic pentacene process which is extensible to other organic materials.

II. Film Growth and Ordering

Pentacene's excellent semiconducting performance is the result of the high degree of molecular ordering seen during its film growth. Once the gate and gate insulator have been deposited in typical laboratory top contact devices, pentacene is evaporated under ultrahigh vacuum conditions in a molecular beam deposition arrangement. Details on the deposition system and process can be found in [6]. Pentacene is a nonpolar rigid short molecule and is repelled by substrates typically used, which are polar (e.g., SiO_2). Pentacene stands almost normal to the substrate and at room temperature packs in a crystalline structure similar to the triclinic structure observed in bulk single crystals [7], [8]. The pentacene layers deposited after the completion of the first polycrystalline layer encounter a different surface energy compared to the first layer deposited on SiO_2. As a result, these layers are less ordered and have smaller grains in a manner similar to Stranski-Krastanov growth. Under specific deposition conditions, they form the "single-crystal phase" of pentacene, as opposed to the "thin film phase" formed directly on SiO_2. These growth forms and processes have been well documented by X-ray diffraction analysis [7], [9]. A typical surface micrograph of pentacene grown on an oxide is shown in Fig. 3.

Metals do not repel pentacene due to their almost infinite ability to rearrange their surface charge to accommodate nearby molecules. The effective surface energy is therefore considerably lower than that of materials typically used for the gate dielectric layers which serve as the substrate for pentacene growth (this effect is reported for poly(a-methylstyrene) in [10]). Normally, higher attraction is expected to lead to smoother and more

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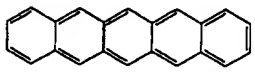

Formula: $C_{22}H_{14}$	[18]
Molecular Weight: 278.35	[18]
Melting Point: 573K	[18]
Vapor Pressure at 444K: 0.00161 Pa	[18]
Optical Bandgap: 2.8 eV	[19]

Fig. 1. Structure and basic properties of pentacene.

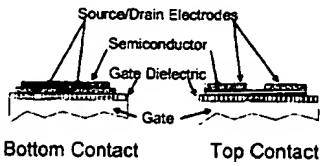

Fig. 2. Transistor layout showing two layout alternatives.

Fig. 3. Micrograph of pentacene grown on typical oxide.

highly ordered growth patterns (see [11] for an example involving amorphous silicon and [12] for an example in a crystalline system). This is not the case with pentacene since repulsion from the substrate is essential for favorably ordered growth. Growth of the large-grained first layer of pentacene is consequently not observed on metals. This type of behavior has been observed in other rigid, short molecule systems, where an attractive surface disrupts the ordered packing of an otherwise crystalline rigid rod structure [13]. Absence of repulsion between the pentacene backbone and the substrate causes a fraction of the admolecules to lie flat on the surface during condensation which prevents lateral ordering, and a different nonplanar form of the material occurs on the metal contact [5]. A micrograph of a typical pentacene layer formed on top of a metal layer is shown in Fig. 4(a). The contrast between the two deposited phases is schematically drawn in Fig. 9.

In an organic FET the structure and contact behavior of the film formed on top of most of the electrode is not important for the performance of the device. Device behavior is only affected by the structure of the material in and immediately bordering the channel. The mobility in the metallic electrode is many orders of magnitude higher than that in the semiconductor, consequently charge injection only occurs at the channel edge. It is the crystalline structure of pentacene at this edge which causes the performance limitation of the bottom contact arrangement. The large grain, well ordered structure in the center of the channel changes into a microcrystalline structure as we move closer to the edge of the channel. Right at the edge of the channel between the interface with the bottom contact electrode is seen an area

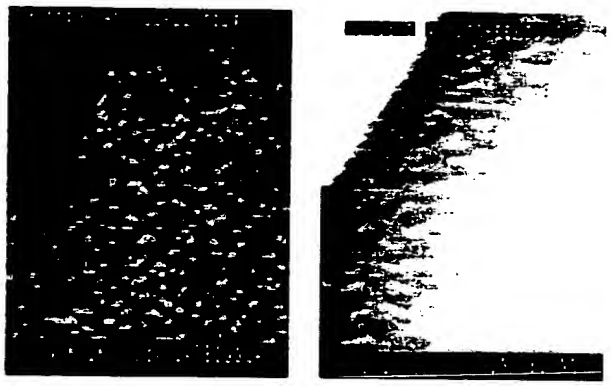

Fig. 4. These micrographs were taken from a bottom contact sample. pentacene was deposited on SiO_2 with patterned Au electrodes on it. (a) Microcrystalline growth of pentacene on Au. The edge of the Au electrode is in the upper-left corner of (b). To the right the large-grained pentacene structure expected toward the center of the channel (on SiO_2) is seen. From the edge of the Au toward the center of the channel a transition region exists containing the microcrystalline form of pentacene. This form is believed to be the cause of inferior performance for bottom contact devices.

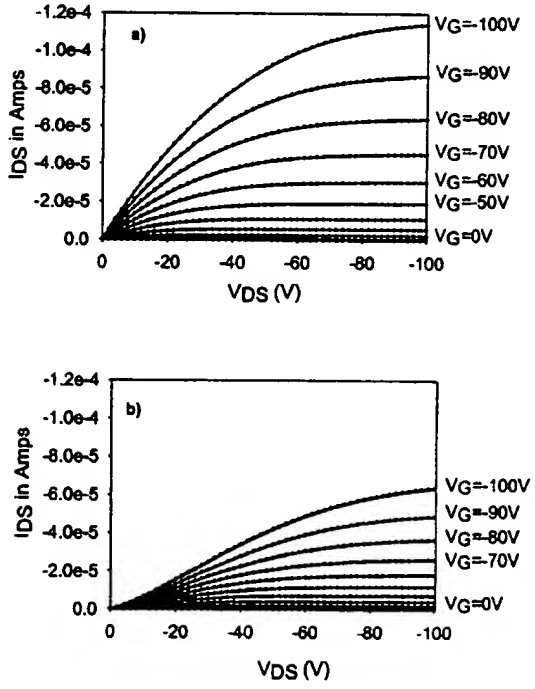

Fig. 5. Performance curves for simultaneously deposited untreated (a) top and (b) bottom contact devices. Both devices are 70 μm $\times$ 1500 μm. The top contact device exhibits superior performance with almost double the mobility and current carrying capability—0.25 cm^2 $(V \cdot s)^{-1}$ versus 0.13 cm^2 $(V \cdot s)^{-1}$. Also note the sigmoidal nonlinear turn-on in the bottom-contact device, which we believe is a product of the nonlinear charge conduction in the trap barrier.

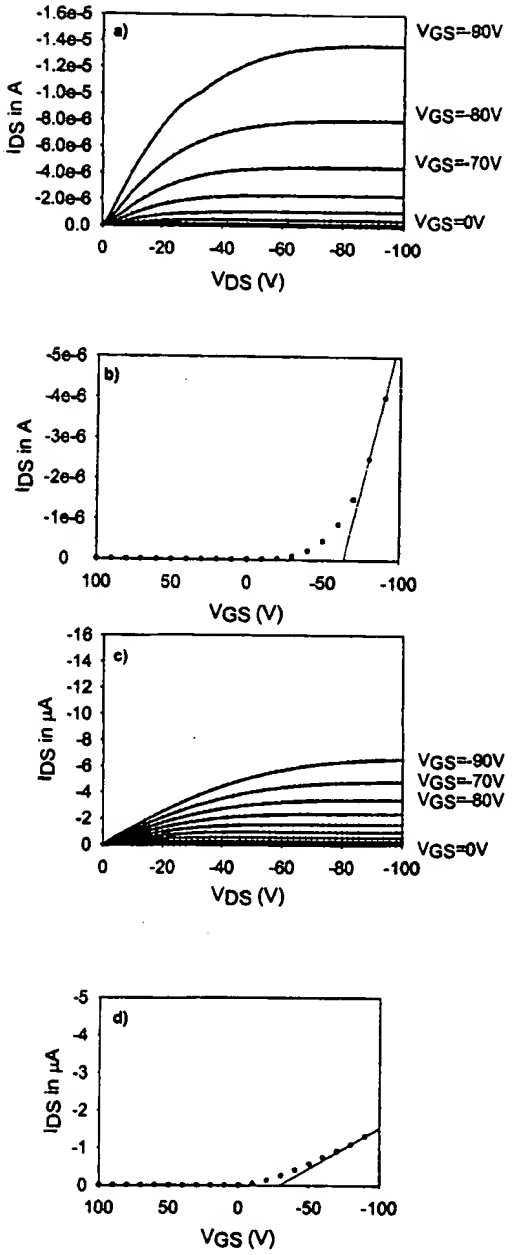

Fig. 6. Linear region I_{DS} versus V_G graphs of treated (a), (b) and untreated (c), (d) devices shown drawn to the same scale for comparison. All devices are 70 μm × 1500 μm. The treated device exhibits significantly higher current carrying ability, and has a mobility of 0.102 cm^2 (V · s)$^{-1}$ in the linear region. The control device, which was soaked in pure ethanol instead of the thiol solution, has a mobility of 0.014 cm^2 (V · s)$^{-1}$ for the treated device and 0.022 cm^2 (V · s)$^{-1}$ for the untreated device. This increase in performance clearly demonstrates the effectiveness of the process.

with a large number of grain boundaries and crystal frustration [Fig. 4(b)].

III. Device Performance

Typical performance curves for top and bottom contact devices are shown in Fig. 5. Excepting the electrode placement, the pairs of devices shown are otherwise identical and were produced simultaneously. The absolute level of mobility varies substantially amongst sample pairs because of variations in the source material. One observed phenomenon is that the first several device runs after loading new source material exhibit poorer performance. High vapor pressure impurities which sublime with the semiconductor material are suspected to cause this problem. Many impurities act as dopants, increasing the parasitic channel conductance (decreasing the on/off ratio), and others act as trap centers which reduce the effective channel mobility. After several runs these impurities are depleted from the source material and performance improves. A number of control sets have confirmed that identical samples produced in the same run have reproducible characteristics.

The behavior observed in the $I-V$ characteristic is what would be typically expected from a field effect transistor. The bottom electrode device exhibits a strong nonlinearity near the origin and conducts significantly less current than expected at low drain-source voltages. It is clear that there is a nonlinear charge injection into the channel occurring. It might initially appear that a Schottky barrier is responsible for this nonlinearity. Gold, however, was used as the electrode for these devices. Au has a high workfunction which has been proven to give good ohmic contact to pentacene.

Several studies have demonstrated that the trap density is significantly higher and performance correspondingly decreased when organic semiconductors have a large number of small grains and many grain boundaries which form trapping sites [14]. The movement of charge carriers through a trap-dense system is impeded by scattering at these traps and momentum transfer of the carriers to phonons in the crystal. This decreases the mobility of the carriers (holes in the case of pentacene) in the material, and macroscopically the increased scattering manifests itself as a decreased field effect mobility in transistors with these increased grain boundary areas. It is believed that this scattering, and its nonlinear relation to electric field, accounts both for the nonlinearity observed at the origin and the lower effective mobility seen in bottom contact devices.

IV. Experimental Procedure

The solution to this problem, therefore, is to increase the ordering of the pentacene on the electrode and at the channel edge. To accomplish this the effective surface energy of the metal must be reduced. Self-assembled monolayers (SAMs) are able to change the polarity (and as a consequence surface energy) of a material by attaching on one end and presenting a backbone chain with selectable characteristics on the other end. Thiol-based SAMs have been extensively studied on metals such as gold and platinum and are well characterized [15]. Indeed, one of the most widely used characterization techniques for self assembled monolayers is the measurement of the surface energy by observing the contact angles of solvents on treated surfaces. Another appealing characteristic of using a SAM is the self-limiting characteristic of such films. Once a monolayer has adhered to the surface no more material will attach. This prevents a thick layer from forming which might interfere with charge injection into the FET channel.

The transistors were fabricated on a degenerately doped silicon wafer, which also served as a gate electrode. A thermally

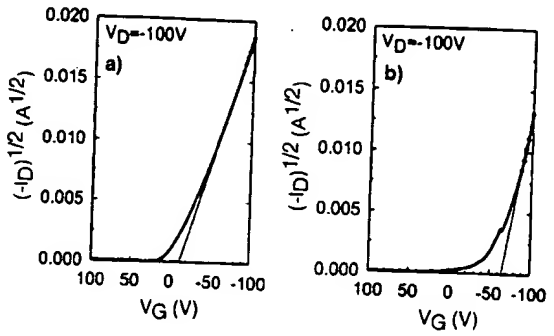

Fig. 7. Saturation region characteristic curves of two samples produced using the process of Fig. 6. Both graphs are on the same scale for comparison. A significantly higher slope and sharper turn-on is seen in the treated sample (b). The device in (a) has a saturation effective mobility of 0.16 cm^2 $(V \cdot s)^{-1}$ with VDS at -100 V, whereas the device in (b) has a mobility of 0.48 cm^2 $(V \cdot s)^{-1}$. The mobility is significantly enhanced by the use of the treatment process—by a factor of 3—even in a situation where the material deposition parameters are very favorable to high performance and the untreated device is performing relatively well.

Fig. 8. Micrograph of thiol treated edge. This image is from a sample [981 112D, discussed in Fig. 7(b)]. A 1-hexadecanethiol SAM was deposited on Au followed by pentacene. The pentacene forms large grains on top of the electrode, which can be seen on the left-hand side of the micrograph, and the grain boundary frustration observed in Fig. 4 is not seen. The lack of small grain structure material in the channel is believed to lead to reduced trap density and the higher performance seen in these devices.

grown silicon dioxide layer was used as the gate dielectric for the transistors. Gold-chrome electrodes were then deposited and patterned on SiO_2 substrates by electron beam deposition The electrodes were patterned using shadow masks for convenience, but nothing prevents the use of lithographically patterned electrodes for this process. 1-hexadecanethiol was applied from solution to the Au-Cr electrodes to modify the surface energy. In this step it is key that chrome or another appropriate material must be used as an adhesion layer for the electrode because the thiol treatment lifts pure gold films from SiO_2.

The thiol was applied by forming a dilute solution of 1-hexadecanethiol in ethanol and immersing the substrates overnight, using part of the procedure from [16]. Pentacene was then evaporated under ultrahigh vacuum conditions onto the electrodes. Device characteristic curves and mobility measurement results for a treated sample and a control which was soaked in pure ethanol prior to deposition are shown in Fig. 6. It can be seen that the treatment increases the mobility considerably—by a factor of 7 in the linear region and more than a factor of 5 in the saturation region—and also increases the current carrying capability of the device considerably. The treated device has performance comparable to top-contact devices using the bottom contact geometry. Great care was taken to eliminate all possible variables in metal deposition, cleaning of the substrate wafers, etc. Both sample substrates were processed simultaneously and in the same deposition runs, with thiol added to the ethanol solution used to treat one of the wafers as the only variable. This result has been repeated with similar success in other sample pairs. Such a pair is shown in Fig. 7. The mobility is enhanced by a factor of 3 in the 1-hexadecanethiol treated sample to 0.48 cm^2 V^{-1} s^{-1} [Fig. 7(b)], even in a situation where the material deposition parameters are very favorable to high performance and the untreated device is performing relatively well ($\mu = 0.16$ cm^2 V^{-1} s^{-1}) [Fig. 7(a)].

It is clear from these measurements that the treated sample has a significantly higher mobility. Scanning electron microscopy also confirms that the samples have significantly

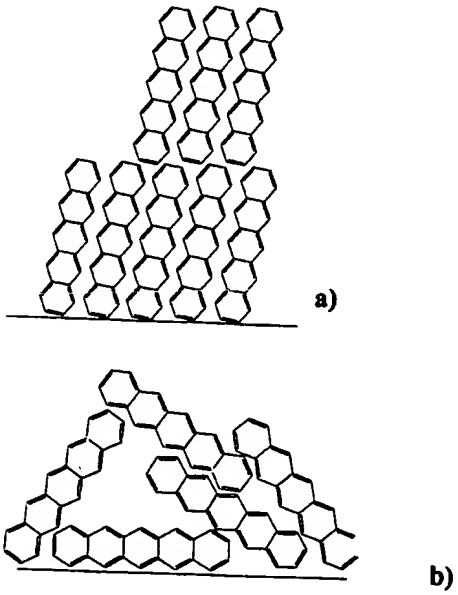

Fig. 9. (a) Schematic diagram of ordered packing state, with substrate repelling pentacene molecules. (b) When the pentacene is attracted to the substrate material, as is the case with metals, the ordered packing state cannot form.

different morphologies. Fig. 8 shows a micrograph of the channel edge of a device formed by depositing pentacene on top of a treated electrode. The structure in this micrograph shows large grains on both sides of the electrode edge, demonstrating that the SAM has led to an increase in the grain size on the electrode. While further tests are needed to directly confirm the hypothesis that the increase in grain size leads to a decrease in trap density and consequently higher performance, this result is fully consistent with the conclusion reached by other studies in which the pentacene grain size has been modulated using

other means, such as by using temperature and deposition rate as in [17].

One open question is the effect on contact resistance of placing a potentially insulating film on top of the electrode. While this is normally expected to increase the contact resistance, the overall effect observed shows significant net benefit to the process. SAMs properly deposited are extremely thin and do not present a significant conduction barrier. Additionally, the effective contact resistance in normal bottom-contact devices is both high and nonlinear. This process eliminates the barrier small grain size semiconducting material presents to charge injection into the channel.

V. Conclusions

This technique has the potential to greatly expand the applicability of organic semiconductors as active elements in dense lithographically patterned circuits. It allows the large grain growth of pentacene seen in the channel center on the SiO_2 gate dielectric to also occur on the electrodes deposited before the semiconductor. The highly ordered structure this forms allows high performing semiconductor material to be grown through the entire channel regardless of the surface energy of the material serving as the deposition substrate. The high performance once limited to devices in which pentacene was deposited on dielectrics only can now be observed in devices where the electrodes are deposited first on the dielectric followed by the pentacene film. This permits photolithography of the electrodes in a high-performance organic FET device and is a key step to producing a manufacturable deposition process for such devices.

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